

## Etched ion tracks in silicon oxide and silicon oxynitride as charge injection or extraction channels for novel electronic structures

D. Fink <sup>a,\*</sup>, A.V. Petrov <sup>a</sup>, K. Hoppe <sup>b</sup>, W.R. Fahrner <sup>c</sup>,  
R.M. Papaleo <sup>d</sup>, A.S. Berdinsky <sup>e</sup>, A. Chandra <sup>f</sup>, A. Chemseddine <sup>a</sup>,  
A. Zrineh <sup>g</sup>, A. Biswas <sup>h</sup>, F. Faupel <sup>h</sup>, L.T. Chadderton <sup>i</sup>

<sup>a</sup> Dept. SF4, Hahn-Meitner-Institute Berlin, Glienicker Strasse 100, Berlin D-14109, Germany

<sup>b</sup> Technical Highschool of South Westfalia, Hagen 58084, Germany

<sup>c</sup> Institute of Electrotechnique, Fernuniversität, Hagen 58084, Germany

<sup>d</sup> Instituto de Física, PUC, Porto Alegre, RS 91500, Brazil

<sup>e</sup> Novosibirsk State Technical University, Novosibirsk 630092, Russia

<sup>f</sup> Institute of Physics, Panjab University, Chandigarh 160014, India

<sup>g</sup> Chemical Institute, University of Rabat, Morocco

<sup>h</sup> Faculty of Engineering, Christian-Albrechts-University, Kiel 24143, Germany

<sup>i</sup> Inst. of Advanced Studies, Australian National University, Canberra ACT 2601, Australia

### Abstract

The impact of swift heavy ions onto silicon oxide and silicon oxynitride on silicon creates etchable tracks in these insulators. After their etching and filling-up with highly resistive matter, these nanometric pores can be used as charge extraction or injection paths towards the conducting channel in the underlying silicon. In this way, a novel family of electronic structures has been realized. <sup>1</sup> The basic characteristics of these “TEMPOS” (= tunable electronic material with pores in oxide on silicon) structures are summarized. Their functionality is determined by the type of insulator, the etch track diameters and lengths, their areal densities, the type of conducting matter embedded therein, and of course by the underlying semiconductor and the contact geometry. Depending on the TEMPOS preparation recipe and working point, the structures may resemble gateable resistors, condensers, diodes, transistors, photocells, or sensors, and they are therefore rather universally applicable in electronics. TEMPOS structures are often sensitive to temperature, light, humidity and organic gases. Also light-emitting TEMPOS structures have been produced. About 37 TEMPOS-based circuits such as thermosensors, photosensors, humidity and alcohol sensors, amplifiers, frequency multipliers, amplitude modulators, oscillators, flip-flops and many others have already been designed and successfully tested. Sometimes TEMPOS-based circuits are more compact than conventional electronics.

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\* Corresponding author. Tel.: +49-30-8062-3029; fax: +49-30-8062-2293.

E-mail address: [fink@hmi.de](mailto:fink@hmi.de) (D. Fink).

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## 1. Introduction

The renaissance of ion track applications that was initiated in the past decade essentially by Martin and his group [1] centered nearly exclusively on the polymers polycarbonate (PC) and polyethylene terephthalate (PET) as base materials. Other track-bearing materials such as cellulose nitrate, polyallyl diglucon (CR39) and mica have hardly been considered for applications in, e.g., electronics or medicine. Possibly useful candidates such as other polymers (polyimides, polysiloxanes, polysilanes) [2–4], diamond [5,6], or fullerene [7–9] (the latter two ones yielding non-etchable tracks with distinct conductivity enhancement), came into focus only recently.

Also silicon oxide and oxynitride fall into the above list of materials that yield processable tracks after swift heavy ion impact (see e.g. Fig. 1). These materials are often found as thin layers on top of silicon wafers, where they serve as dielectric media for MOS structures etc. Usually, heavy ion irradiation of such oxide- or oxynitride-containing electronic devices leads to a deterioration of their electronic properties, degrading sophisticated silicon-based structures in extreme cases to simple resistances. Therefore the initial enthusiasm in the 50s and 60s of the last century about swift heavy ion irradiation of silicon-based electronics for device improvement faded rapidly, and today heavy

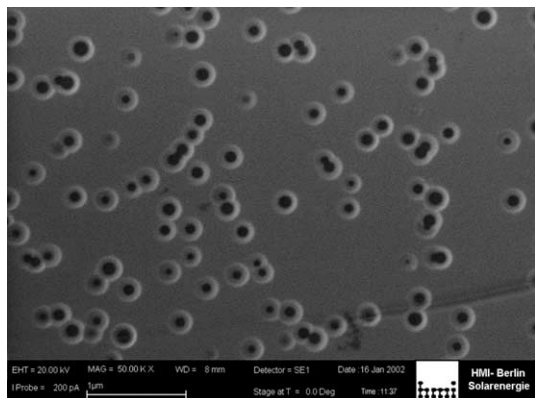


Fig. 1. SEM images of etched ion tracks in thermally grown  $\text{SiO}_2$  on Si. Layer thickness about 200 nm, etching in 4% HF at RT for a few min.

ion irradiation of electronic structures is essentially only used to control their radiation hardness.

In this paper we introduce a family of new electronic structures which makes distinct use of etched tracks in their dielectric layers. Therefore we called this family by the acronym “TEMPOS”<sup>2</sup> which stands for “Tunable Electronic Material with Pores in Oxide on Silicon” – the pores being the etched ion tracks. In this paper we shall outline the general construction principle of TEMPOS elements and show their most basic characteristics. More detailed reports, especially on TEMPOS applications, will be published separately [10].

## 2. The construction of TEMPOS structures

The three new basic ideas of the TEMPOS concept (Fig. 2) are:

- (a) to replace the metallic gate electrode on top of the dielectric layer of conventional MOS-FET structures [11] by a highly resistive layer **L** that connects both surface contacts. In that way, the potential distribution of the device – and hence also the overall charge carrier distribution – is altered, especially in the interface-near silicon channel **C**.
- (b) to insert etched ion tracks **T** within the oxide layer of MOS devices and to fill them with highly resistive matter. In this way, additional paths for charge extraction or injection between the conducting channel **C** in the silicon and the top resistive layer **L** on the oxide surface are formed that are absent in the classical MOS-FET concept. This leads partly to dramatic deviations of the charge carrier distribution from anything known.
- (c) to add a base electrode for controlling the device’s functionality. That concept dates back to

<sup>2</sup> Our original intention to use the acronyms: “TOSCA” (for: “Tracks in Oxide on Silicon for Charge Applications”) or “POSE” (for “Pores in Oxide on Silicon for Electronics”) for that device could not be realized as these names were already protected.

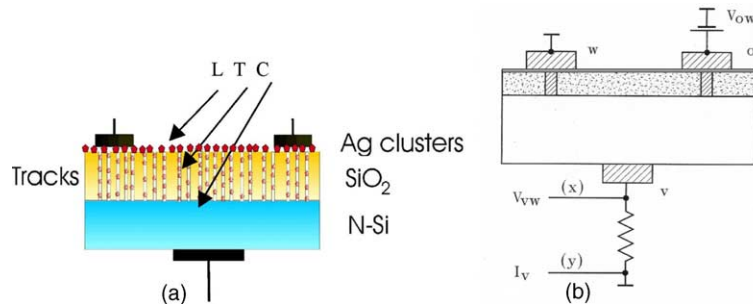


Fig. 2. (a) Principle sketch of a TEMPOS element (shown here with metallic nanocluster filling of tracks and on surface); (b) the TEMPOS symbol and its usual wiring. L: poorly conducting surface layer; T: conducting pores (such as filled etched tracks); C: conducting silicon channel below interface.

the beginning of MOS-FET research [11] but was often abandoned later. In FET's, the effect of such a base electrode is similar as that one of a gate electrode.

N- and p-type silicon wafers of  $\sim 300 \mu\text{m}$  thickness and of resistivities between  $0.005$  and  $35 \Omega\text{cm}$ , cut in  $[111]$  or  $[100]$  direction, were used as carrier materials. They were cleaned as usual and then oxidized in dry atmosphere, to form dielectric layers of some  $100 \text{ nm}$  thickness. Alternatively, silicon oxynitride ("SiON") layers of  $\sim 50 \text{ nm}$  to  $2 \mu\text{m}$  thickness were deposited onto the Si wafers by means of plasma chemical vapor deposition (PCVD). After protecting the top layers by a spin-coated and baked photoresist film, the oxide of the rear side was etched away with commercial ammoniacal fluoride etchant solution. Thereupon an Al layer was electron-gun evaporated onto the rear side to serve as the base contact, denoted by "v" in Fig. 2(b).

Subsequently the surface protection was removed and the samples were exposed to ion irradiation of  $2 \times 10^8 \text{ cm}^{-2}$  Au ions of  $20 \text{ MeV}$  energy at the accelerator of Buenos Aires University, Argentina, or of  $(1 \text{ to } 5) \times 10^8 \text{ cm}^{-2}$  Xe or Au ions at  $300\text{--}400 \text{ MeV}$  at the swift heavy ion accelerator "ISL" of the HMI Berlin, Germany. The applied fluences are chosen so that even after subsequent ion track etching (with  $4 \text{ at}\%$  HF up to  $10 \text{ min}$  for SiO<sub>2</sub> and  $40 \text{ at}\%$  HF up to  $7 \text{ min}$  for SiON) the resulting pores do not yet overlap. These pores (or "etched tracks") are cylindrical for SiON with typical diameters around  $\sim 300 \text{ nm}$  (not shown

here) and conical in shape for SiO<sub>2</sub> with  $\sim 250 \text{ nm}$  at the surface and  $\sim 150 \text{ nm}$  at the Si interface (Fig. 1).

In the next step, a thin layer L of a material with high electrical resistivity such as e.g., fullerite (C<sub>60</sub>) or phthalocyanine was deposited onto the surface of the dielectric layer and in the interior of the etched tracks. The material and its thickness were chosen so to obtain some  $\text{M}\Omega$  to  $\text{G}\Omega$  between the surface contacts "o" and "w" (see below), and usually some  $\text{k}\Omega$  to  $\text{M}\Omega$  along the tracks.

Alternatively, we have prepared layers of dispersed nanoclusters of metals or semiconductors such as Ag, Au, CdS, PbS, TiO<sub>2</sub>, or others. These clusters with typical diameters in the  $\sim 5$  to  $\sim 50 \text{ nm}$  range have either been directly deposited onto the dielectric surfaces, or they were embedded in somewhat thicker layers of insulating or weakly conducting polymers such as teflon or polyethylene oxide (PEO), respectively, with typical cluster-to-cluster distances in the order of  $\sim 10$  to  $\sim 100 \text{ nm}$ . Whereas in the corresponding metallic bulk materials the conductivity stems from electrons in the conduction band, the conduction mechanisms of such dispersed clusters changes via electron tunneling processes to, e.g., Schottky emission or field emission with increasing distances between the nanoparticles, depending on the voltage applied. Eventually, in the latter case also some ionic conductivity might contribute stemming from residual traces of the etchant or from surface contaminations by aerosols (these first examinations were not yet performed in cleanrooms), combined with atmospheric moisture. Such nanoclustered

layers can be easily tailored to obtain any resistivity value between insulating and conducting, by varying the cluster-to-cluster distance.

In a last step the sample surface layer **L** was contacted at two positions “*o*” and “*w*” spaced by a few mm from each other. For simplicity, we used commercial conducting silver paste in these test experiments. Fig. 2(a) gives the principle sketch of the thus obtained arrangement, and Fig. 2(b) shows how this device is usually electrically connected.

### 3. The electronic behavior of TEMPOS structures

The current–voltage measurements were usually performed between *o* and *v* whereas the contact *w* was usually kept at ground potential. Figs. 3(a) and (b) show the principle DC characteristics of TEMPOS structures. Depending on the track resistivity, two nearly complementary  $I/V$  characteristics emerge. In the given example, the track resistivities were obtained by filling nanoclusters of the same size distribution and same average cluster-to-cluster distances into tracks that were etched for different times (i.e. up to narrow and wide diameters, respectively.) It appears that, whereas the Type 1 devices (etching from 3 to 5 min) are only little influenced by charge extraction from the silicon channels, the Type 2 devices (etching from

7 to 10 min) are dominated by that effect. Whereas the characteristics of Type 1 structures resembles somewhat that one of pnp transistors, Type 2 structures rather are of npn type. This signifies that track conductivity variations (i.e. control of charge extraction from, or injection into the channel) enables one to obtain the same effect (the inversion of the  $I/V$  characteristics) that in conventional electronics requires adequate alteration of the semiconductor doping.

Due to their symmetric construction, the contacts *o* and *w* are, in principle, interchangeable. Furthermore, if the overall electric resistance along the tracks is chosen to be similar in its order of magnitude as that one on the surface between the contacts *o* and *w*, then there is also an astonishingly close similarity obtained between the electrical characteristics when interchanging the top contacts *o* or *w* with the base contact *v* in electronic circuits, Fig. 4.

TEMPOS structures are found to be rather stable even under some electrical load. For example, devices consuming some 10 mW (operating at, e.g.,  $V_{vw} = 60$  V and  $V_{ow} = 15$  V at a temperature of  $\sim 40$  °C) are stable in their characteristics for days to weeks. As at more elevated temperatures corrosion and/or oxidation of the conducting layer might modify the device response such possibly destructive experiments have not yet been performed.

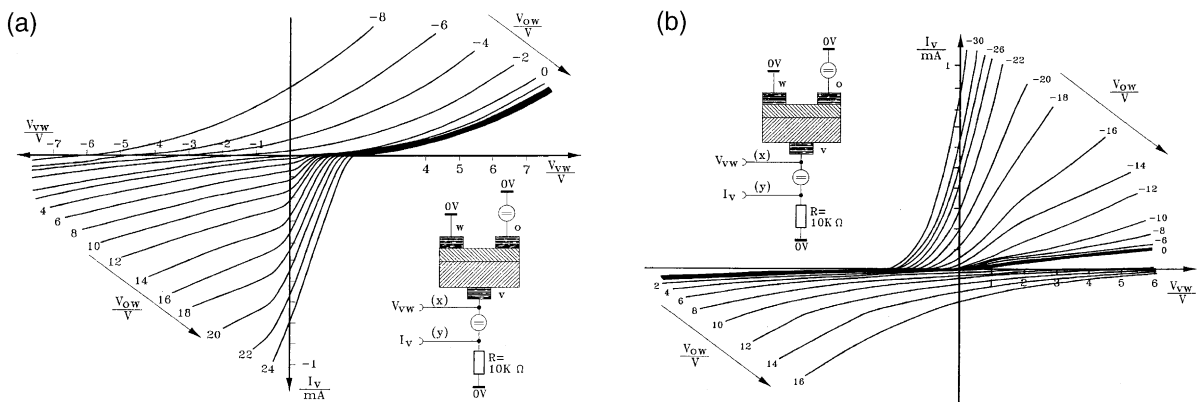


Fig. 3. The two typical DC current/voltage characteristics of a TEMPOS device. (a) Type 1, (b) Type 2. The  $I/V$  curves are smoothed to outline the principle behavior better. The corresponding wiring is also shown.

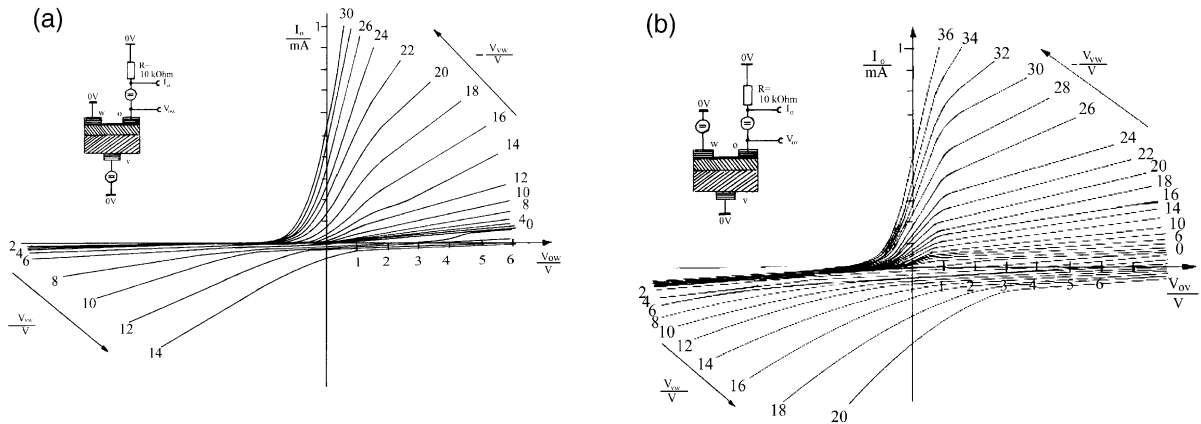


Fig. 4. The DC current/voltage characteristics of a Type 2 TEMPOS device, shown for (a)  $I_o(V_{ov})$  with parameter  $V_{vw}$  and (b)  $I_o(V_{ov})$  with parameter  $V_{vw}$ . For the third possibility,  $I_v(V_{vw})$  with parameter  $V_{ov}$ , see Fig. 3(b). The  $I/V$  curves are smoothed to outline the principle behavior better.

If, under else identical conditions, the tracks in the TEMPOS structures are missing or existing latent tracks are not etched, then no such characteristics are recorded; instead one gets a linear  $I/V$  relation describing the highly resistive surface coverage only. If etched tracks exist in the dielectric layer that are not filled with weakly conductive matter, no current is recorded at all for whatever applied voltage, and if the tracks and surfaces are covered with highly conductive matter, then the whole structure is just shortcut. All these findings indicate that TEMPOS structures are not just modified MOS-FETs but virtually new electronic devices that differ distinctly from existing ones.

The theory of TEMPOS structures is still at its beginning, but some parts of their  $I/V$  characteristics are already understood [10]. In contrast to conventional transistors, TEMPOS structures have additional free parameters such as the etched track density, position, length, diameter and shape, and the type of matter embedded in these tracks and on the surface, which gives a large variation of possibilities resulting in partly unconventional new properties. This means that TEMPOS is not just one single new electronic structure but a whole new electronic family.

As a general rule, we may state that the higher internal complexity of TEMPOS structures as compared with conventional electronic elements

allows one to design TEMPOS-containing circuits with greater simplicity. The reduction in the number of peripheric elements for wiring a given circuit leads to a gain in operation speed – hence to the inherent feasibility of TEMPOS circuits for high frequency operation. Though we restricted our first TEMPOS examinations essentially to DC or very low frequencies, we have got already first hints for the feasibility to operate TEMPOS devices also in the MHz regime. By reducing the TEMPOS structure size from at present  $\sim 5 \text{ mm} \times 5 \text{ mm}$  to a few  $\mu\text{m}^2$  or less (corresponding to the area occupied by two ion tracks), we expect further considerable increases in operation frequency.

TEMPOS structures are also expected to be inherently radiation-hard electronic elements, as the transient addition of a few radiation-induced discharge channels to some  $\sim 10^8$  already existing charge transfer channels (i.e. the etched tracks) should not alter the overall device characteristics markedly. Especially the highly resistive top and track connections should dampen the effect of any sudden transient shortcut.

The use of nanoclusters for the design of highly resistive layers in TEMPOS structures enables one to exploit additionally their optical and charge-transfer properties so that one can create a number of new optoelectronic devices. For example, one might make use of the emission of point-like

sparkling light in all colors that was found in suitable configurations. The light emission was found to be reproducible and stable within a few months. Light emission has been observed hitherto only in TEMPOS structures with etched tracks filled with silver nanoparticles. The light emission is more pronounced for tracks in SiON than in SiO<sub>2</sub>. This can possibly be attributed to the photoluminescent properties of SiON. The power of the emitted light in the first case was measured to be 190 pW for ~200 point-like light sources upon a current  $I_v = 5$  mA and 1.36 nW at  $I_v = 15$  mA. Assuming that the ~5 nm large silver clusters were responsible for that light emission, the emitted power density would be as large as ~30 W/cm<sup>2</sup>.

TEMPOS structures with fillings of TiO<sub>2</sub> nanoclusters, {Au nanocluster/teflon} composites, or {CdS nanocluster/PEO} composites did not yield any non-zero DC characteristics, however at AC frequencies the structures start operating. If thicker layers of isolated nanoclusters (e.g., {semiconductor nanocluster/polymer} composites) are deposited onto the TEMPOS structures, the AC  $I/V$  characteristics exhibit hystereses, due to the polarization of the deposited conducting material. If the highly resistive material is replaced by fullerite, strongly humidity-, alcohol-, acetone- and light sensitive TEMPOS structures emerge. Phthalocyanine filling yields similar effects.

Depending on the specific TEMPOS property under consideration, corresponding demonstration devices have been built from TEMPOS structures that can be used as switches, low frequency noise generators, optoresistive and optocapacitive sensors, optocapacitive remote control of local oscillators and band, high or low passes, signal frequency multipliers, amplitude modulators, thermocapacitive and thermoresistive sensors, astable multivibrators, phototransistors and optoelectronic light-emitting nanodevices, amplifiers, oscillators and others.

#### 4. Conclusions

We have introduced a new concept in electronics, which is the use of etched ion tracks in a dielectric layer on top of silicon, in order to extract

or to inject charge carriers in well-defined regions of MOS structures. This approach leads to a whole family of novel electronic elements which we denoted as “TEMPOS” = tunable electronic material with pores in oxide on silicon. In spite of some similarity with known electronic elements, their overall behavior makes them distinctly different from anything that is known in electronics up to now. Their principle advantage in comparison to “classical” structures [11] is their higher complexity, that implies greater flexibility and greater simplicity in designing electronic circuits, and probably higher operation speed. In principle, TEMPOS structures can be miniaturized up to at least the micrometer scale.

Some ~35 electronic circuits have already been designed successfully with different TEMPOS structures, and many more appear feasible. Specifically we think that the incorporation of environmentally sensitive materials will lead to a multitude of sensor applications. Conductive, resistive and capacitive TEMPOS sensors can be developed. Suitable multicontacting combined with careful suppression of cross-talking enables one to perform parallel data processing with one TEMPOS element only.

The driving force of technological development is money. The additional irradiation step required for TEMPOS structures will cost between ~10 cents and 1 € (or US \$) for a 10 cm  $\varnothing$  wafer with 10<sup>8</sup> tracks/cm<sup>2</sup> from which at least some hundred to thousands of elements can be cut. In comparison with the other production costs, this amount is negligible. The production of TEMPOS structures is easier and cheaper than that of conventional electronics insofar as usually they do not require cleanroom conditions.

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## References

- [1] C.R. Martin, *Science* 266 (1994) 1961, and many references cited therein.
- [2] R. Spohr, *Ion Tracks and Microtechnology*, Vieweg, Braunschweig, 1990.
- [3] D. Fink, R. Klett, *Braz. J. Phys.* 25 (1995) 54.
- [4] D. Fink (Ed.), *Ion Irradiation of Polymers: Fundamentals and Applications*, Springer, Berlin/Heidelberg, 2003.
- [5] D. Fink, L.T. Chadderton, S.A. Cruz, W.R. Fahrner, V. Hnatowicz, E.H. te Kaat, A.A. Melnikov, V.S. Varichenko, A.M. Zaitsev, *Radiat. Eff. Def. Solids* 126 (1993) 247.
- [6] J. Krauser, A. Weidinger, J.H. Zollondz, B. Schultrich, H. Hofsäss, B. Ronning, in: *Proc. Workshop on the European Network on Ion Track Technology*, Caen, France, 24–26 February 2002.
- [7] A.S. Berdinsky, D. Fink, A.V. Petrov, M. Müller, L.T. Chadderton, J.F. Chubaci, M.H. Tabacniks, *MRS Boston Fall Meeting 2001 Boston 27 November–1 December 2001*; Contribution Y4.7.
- [8] A.S. Berdinsky, D. Fink, H.G. Chun, L.T. Chadderton, P. Aleagonkar, in: *Proc. Seventh Korean–Russian Meeting*, Ulsan University, Korea, 30 June–3 July 2003.
- [9] A.S. Berdinsky, D. Fink, H.G. Chun, L.T. Chadderton, A.V. Petrov, P. Aleagonkar, in: *Proc. Seventh Korean–Russian Meeting*, Ulsan University, Korea, 30 June–3 July 2003.
- [10] D. Fink, A. Petrov, W.R. Fahrner, H. Hoppe, A.G. Ulyashin, R.M. Papaleo, in: *Proc. ISEC*, Peking, China, 2003.
- [11] P. Richman, *Characteristics and Operation of MOS Field Effect Devices*, Mc Graw-Hill, New York, 1967.